APPLICATION FOR UNITED STATES PATENT

in the name of

Michael G. Adlerstein

Of

Raytheon Company

For

AN INTEGRATED THERMAL SENSOR FOR MICROWAVE TRANSISTORS

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TECHNICAL FIELD

[0001] This invention relates to microwave transistors, and more particularly to circuitry for monitoring temperature of such transistors.

BACKGROUND

[0002] As is known in the art, it is desirable to monitor the temperature of microwave transistors relative to ambient temperature. By monitoring the temperature of such transistors in a monolithic integrated circuit it is possible to (1) insure that the transistor does not exceed a specified temperature over a wide range of operating temperatures; and (2) use the temperature to dynamically tune a circuit having the transistor.

SUMMARY

[0003] A circuit for determining temperature of an active semiconductor device disposed on a semiconductor substrate and a Wheatstone bridge circuit. The bridge has in each of four branches thereof a thermal sensitive device, one pair of such thermal sensitive devices being in thermal contact with an electrode of the active device. Another pair of such thermal sensitive devices is in thermal contact with the substrate. The thermal sensitive devices are resistors. The active device is a transistor. A tuning circuit is coupled to an output of the transistor, such tuning circuit having a tunable element controlled by a control signal fed to such tunable element. A processor is responsive to a voltage produced at an output of the bridge circuit and a signal representative of power fed to the transistor. The output provided by the Wheatstone bridge provides a measure of a temperature difference between the temperature of the transistor and ambient temperature. The processor produces the control signal to maximize power fed to the transistor and minimize power dissipated by such transistor.

[0004] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0005] FIG. 1 is a schematic diagram of a circuit for determining the operating temperature of an active semiconductor device according to the invention;

[0006] FIG. 2A is a plan view of a portion of a semiconductor substrate, such portion having a transistor used in the circuit of FIG. 1 thereon and having a four resistors used in the circuit of FIG. 1;

[0007] FIG. 2B is a cross sectional view of the portion of the substrate of FIG. 2A, such cross section being taken along line 2B-2B of FIG. 2A; and

[0008] FIG. 2C is a cross sectional view of the portion of the substrate of FIG. 2A, such cross section being taken along line 2C-2C of FIG. 2A.

[0009] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0010] Referring now to FIG. 1, a circuit 10 is shown for determining the operating temperature of an active semiconductor device, here a transistor 12. The circuit 10 a semiconductor substrate 14 (FIGS. 2A, 2B and 2C) having thereon the active device 12. Here the transistor 12 is a field effect transistor having source electrode, S, drain electrode D and gate electrode G, as shown.

[0011] The circuit 10 includes a bridge circuit 16, here a Wheatstone bridge. The bridge 16 includes a first thermal sensitive device, here a resistor R1, disposed in thermal contact with an electrode, here the source electrode, S, of the active device 12. The first thermal sensitive device R1 has a pair of terminals, a first one of the pair of terminals being connected to a first node N1 and a second one of the pair of terminals being connected to a second node N2.

[0012] The bridge 16 includes a second thermal sensitive device, here a resistor R2, disposed in thermal contact with the source electrode, S, of the active device 12. The second thermal sensitive device R2 has a pair of terminals, a first one of the pair of terminals being connected to a third node N3 and a second one of the pair of terminals being connected to a fourth node N4,

[0013] The bridge 16 includes a third thermal sensitive device, here a resistor R3, disposed in thermal contact with the substrate 14. The third thermal sensitive device R3 has

a pair of terminals, a first one of the pair of terminals being connected to the second node N2 and a second one of the pair of terminals being connected to the fourth node N4.

[0014] The bridge 16 includes a fourth thermal sensitive device, here a resistor R4, disposed in thermal contact with the substrate 14. The fourth thermal sensitive device R4 has a pair of terminals, a first one of the pair of terminals being connected to the first node N1 and a second one of the pair of terminals being connected to the third node N3.
A dc voltage potential 20 is connected between the first node N1 and the fourth node, N4, here such node N4 being at ground potential, as indicated. The second node N2 and the third node N3 provide an output of the bridge 16.

[0015] The circuit 10 includes a tuning circuit 22 coupled to an output electrode of the transistor 12. The tuning circuit 12 has a tunable element 24, here a varactor, controlled by a control signal fed to such tunable element 24 by a processor 26.

[0016] The output voltage between nodes N2 and N3 is proportional to the difference between the product of the resistance of resistor R3 and the resistance of resistor R4 and the product of the resistance of resistor R2 and the resistance of resistor R1. That is, the output voltage between nodes N2 and N3 is proportional to R3R4-R2R1. Resistors R3 and R4 are in thermal contact with the substrate 14 and are thus at a common temperature representative of the ambient temperature of the circuit 10. Resistors R1 and R2 are in thermal contact with the source electrode, S. of the transistor 12. Thus, if the temperature of the transistor 12 and the ambient temperature are the same, as when the transistor is not operating, the output voltage of the bridge is zero. It follows then that when the transistor operates, it will become hotter than the ambient temperature and the output voltage between nodes N2 and N3 will increase. Because the resistance of the resistors R1 and R2 increase with an increase in temperature, it follows then that the output voltage of the bridge 16, i.e., the voltage between nodes N2 and N3, provide a measure of the power being dissipated by the operating transistor 12.

[0017] The processor 26 responsive to the voltage produced at the output of the bridge 16 and a signal representative of power fed to the transistor 12. Any one of a variety of means may measure the power fed to the transistor 12, here, for example, such power is measured by a voltage V produced across a precision resistor R in the source circuit of the transistor 12. The voltage across this resistor is IR while the bias power into the transistor is this current multiplied by the voltage drop across the transistor.

[0018] The processor is programmed to produce the control signal for the varactor which maximizes power fed to the transistor, as detected by the voltage produced across resistor R while minimizing power dissipated by such transistor, as detected by the output voltage across nodes N2 and N3 of bridge 16.

[0019] More particularly, the process of self-alignment and dynamic tuning can be understood based on the following balance equation:

$P_{rf.load} + P_{rf,.tunrers} = P_{dc} - P_{diss} + P_{rf.in}$

where $P_{rf.load}$ is the power to the load, here represented in FIG, 1 by resistor Rl;

$P_{rf,.tunrers}$ is the power dissipated in the tuner 22;

P_{dc} is the power fed to the transistor 12;

P_{diss} is the power dissipated in the transistor as represented by the output voltage of the bridge 16 (i.e., the voltage between nodes N1 and N3); and

$P_{rf.in}$ in the input radio frequency (rf)power fed to the gate G of transistor 12.

[0020] Here, the rf power output is divided into two parts; one is the part that flows into the load; and the other is the part that is dissipated in the tuner 22. The right side of the equation represents the remaining power of the device: the DC bias power (i.e., P_{dc}); the power dissipated as heat and is thus proportional to the temperature rise of the transistor 12; and the rf power input to the transistor 12. For simplicity, the following assumptions are made: (1) the rf power input to the transistor 12 is fixed; (2) the transistor input remains matched over a range of output tuner 22 operating range; and (3) the tuner 22 is lossless such that $P_{rf,tuner}$ is zero.

[0021] With such assumptions, with the circuit 10 (FIG. 1), the use of an rf detector on the output of the transistor is avoided by providing a sensor for P_{dc} and $P_{diss.}$ Here, the sensor for P_{dc} is the resistor R and the sensor for P_{diss} is the bridge 16. It is assumed that the DC voltage across the transistor is fixed.

[0022] Referring now to FIGS. 2A-2C, the substrate 14, here for example silicon or gallium arsenide, has disposed on a source electrode S of the transistor 12 a thin insulating layer, 30, here for example silicon nitride. Disposed on the layer of silicon nitride are evaporated thin film resistors R1 and R2, here made of nichrome, for example. It is noted that when the layer 30 is formed on the source electrode S, a layer 30 of silicon nitride is also formed on portions of the substrate 12.

[0023] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS: